CROSSTALK NOISE AVOIDANCE IN VLSICIRCUITS USING FIBONACCI NUMERAL CODES

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ABSTRACT

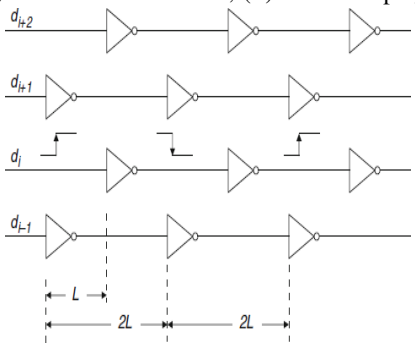
To increase the interconnect resistance, length, and inter-wire capacitance we are going with deep sub micrometer CMOS process technology which contribute to large on-chip propagation delay. When the data is being transmitted over interconnect determine the propagation delay where the delay is observed to be extremely significant when adjacent wires are transitioning in opposite directions (i.e; crosstalk transitions) as compared to transitioning within the same direction. As a result, the degradation of high-speed digital circuits thanks to crosstalk. Crosstalk can be defined to be a phenomenon by which logic transmitted in vlsi circuit or net/wire creates undesired effect on the neighboring circuit or nets/wires. Thanks to capacitive coupling as the reduction of crosstalk has become more important for the high-speed digital circuits. We are reducing the crosstalk by exploiting Fibonacci number system. We propose a family of Fibonacci coding techniques for crosstalk avoidance relate them to a number of the prevailing crosstalk avoidance techniques by using the CADENCE TOOLS and simulate the codes for the reduction of crosstalk.

Keywords: On-chip bus, crosstalk, Fibonacci coding.

INTRODUCTION

The headway of extremely enormous scope incorporation (VLSI) advancements has been adhering to Moore's law for as far back as quite a few years: the measure of transistors on a microcircuit is multiplying like clockwork and along these lines the channel length is scaling at the speed of 0.7/3 years. It had been in a matter of seconds prior when VLSI configuration walked into the domain of Deep Submicron (DSM) forms, where the base element size is well beneath 1 μm. These propelled forms empower creators to execute quicker, greater and progressively complex plans. With the ascent in intricacy, System on Chip (SoC), Network on Chip (NoC) and Chip-level Multiprocessing (CMP) based items are currently promptly accessible commercially. Some significant difficulties in DSM advancements incorporate plan profitability, manufacturability, power utilization, dispersal and interconnect delay. High plan cost and long pivot time are frequently brought about by the development in structure unpredictability. A high plan unpredictability results from a development in transistor tally and speed,interest for expanding usefulness, minimal effort necessities, brief timeframe to showcase and in this manner the expanding coordination of inserted simple circuits and recollections. Poor manufacturability is generally quick consequences of decrease in include size. Since the component size gets littler, the arranging turns out to be touchy to process variety, which significantly influences yield, unwavering quality and testability. to manage these issues, new structure streams and procedures are actualized to upgrade the proficiency of the plans. IC foundries are adding more structure rules to improve the arranging power. For a few high densities, a fast DSM configuration, power utilization might be a significant concern. Expanding transistor checks, chip speed, and more prominent gadget spillage are driving up both dynamic and static force consumption. In the in the interim, be that as it may, DSM advancements likewise present new difficulties to creators on numerous different fronts like (I) scale and intricacy of

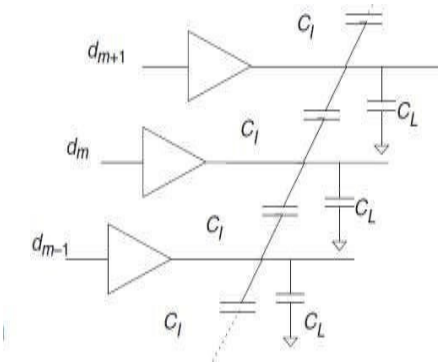
plan, confirmation and test; (ii) circuit displaying and (iii)



handling and manufacturability. Imaginative methodologies are required at both the framework level and in this manner the chip level to manage these difficulties and moderate the negative impacts they convey.

II. ON-CHIP CROSSTALK AVOIDANCE

Capacitive crosstalk has become a significant determinant of the absolute force utilization and deferral of on-chip transports. Figure.1 represents a rearranged on-chip transport model with crosstalk. In the figure, CL means the heap capacitance, which incorporates the beneficiary door capacitance and furthermore the parasitic wire-to-substrate parasitic capacitance. CI is the between wire coupling capacitance between adjoining signal lines of the transport. Practically speaking, this transport structure is commonly demonstrated as a disseminated RC arranges which incorporates the non-zero opposition of the wire too It has been indicatedthat for DSM forms, CI is a lot more noteworthy than CL. In light of the vitality utilization and postpone models given in the transport vitality utilization can be determined as a component of the all out crosstalk over the whole transport. The most pessimistic scenario delay,



which decides the greatest speed of the transport, is restricted by the most extreme crosstalk that any wire in the transport brings about. It has been indicated that diminishing the crosstalk helps the transport execution essentially various methodologies have been proposed for crosstalk decrease with regards to transport interconnects. A few plans center around decreasing the vitality utilization, some attention on limiting the postponement and different plans address both.

Figure 1 simplified on-chip bus model with crosstalk

The most straightforward way to deal with address the between wire crosstalk issue is to shield each flag utilizing grounded channels. Khatri et al. in [1, 2] proposed a design texture that on the other hand embeds one ground wire and one force wire between each sign wire, i.e., the wires are spread out as . . . VSGSVSGSVS . . . , where S signifies a sign wire, G means a ground wire and V indicates a force wire. Any sign wire has a static (V or G) wire on each side, and subsequently, when it switches, it needs to charge a capacitance of estimation of 2CI .

Figure 2 A Fabric Based Design

This texture likewise upholds a structure decide that metal wires on a given layer run opposite to wires on layers above or beneath. The texture has the benefit of improved

$$f_m = \begin{cases} 0 & \text{if } m = 0, \\ 1 & \text{if } m = 1, \\ f_{m-1} + f_{m-2} & \text{if } m \geq 2. \end{cases}$$

consistency in parasitic capacitance and inductance. It consequently gives a low obstruction force and ground organizes also. Such a texture brings about a reduction in wiring thickness. Despite the fact that the texture seems to require a huge zone overhead, exploratory outcomes show that by and large, the circuit size develops by just 3% if the circuit is executed as a system of medium-sized programmable rationale exhibits (PLAs). In the worst case, be that as it may, the circuit size can be more than 200%of the customary format. Figure 2 outlines such a texture based plan. Khatri et al. [1] likewise gives conversations on wire evacuation in systems of Programmable Logic Arrays (PLA).

Crosstalk evasion transport encoding procedures control the info information before transmitting them on the transport. Transport encoding can take out certain bothersome information designs and along these lines diminish or take out crosstalk, with much lower region overhead than the previously mentioned clear protecting strategies. These kinds of codes are alluded to as crosstalk shirking codes (CACs) or self protecting codes. Relies upon their memory prerequisites, CACs can be additionally separated into two classifications: memory less codes and memory-based codes. Memory based coding approaches create a code word dependent on the recently transmitted code and the present information word to be transmitted [34, 100]. On the beneficiary side, information is recuperated dependent on the got code words from the present and past cycles. The memory less coding approaches utilize a fixed code book to create code words to transmit. The code word is exclusively reliant on the info information. The decoder in the beneficiary uses the current got code word as the main contribution to request to recoup the information.

Among all the memory less CACs proposed, two sorts of codes have been vigorously examined. The first is called illegal example free (FPF) code and the second sort of code has the property that between any two contiguous wires in the transport, there will be no change in inverse ways in a

similar clock cycle. Various names have been utilized in the written works for the second sort of codes. Right now, elude these codes as illegal change frees (FTF) CACs. Both FPF-CACs and FTF-CACs yield a similar level of defer decrease as detached protecting while at the same time requiring significantly less territory overhead. Hypothetically, the FPF-CAC has somewhat better overhead execution that the FTF-CAC. By and by, for enormous size transport, this distinction is immaterial.

III. FIBONACCI BINARY NUMERAL SYSTEM

A numeral framework is "where numbers are spoken to by numerals in a predictable way" [5]. The most normally utilized numeral framework in advanced plan is the twofold numeral framework, which uses forces of two as the premise. For a number v, its twofold portrayal is characterized in Eq. 1. The parallel numeral framework is finished and unambiguous, which implies that each number has one and only one portrayal in the double numeral framework.

Equation 1

The Fibonacci-based numeral framework N (Fm, {0, 1}) is the numeral framework that utilizes Fibonacci arrangement as the premise. The meaning of the Fibonacci grouping [3] is given in Eq. 2. A number v is spoken to as the summation of some Fibonacci numbers, and no Fibonacci number is in the summation

$$v = \sum_{k=1}^{n} b_k \cdot 2^{k-1} \qquad b_k \in \{0,1\}$$

$$= \sum_{k=1}^{m} d_k \cdot f_k \qquad d_k \in \{0,1\}$$

more that once, as demonstrated in Eq. 2.

Equation 2

```
\\ MSB stage:
if v ≥ f_{m+1} then
    d_m = 1;
    r_m = v − f_m;
else
    d_m = 0;
    r_m = v;
end if
\\ other stages:
for k = m-1 to 2 do
    if r_{k+1} ≥ f_{k+1} then
        d_k = 1;
    else if r_{k+1} < f_k then
        d_k = 0;
    else
        d_k = d_{k+1};
    end if
    r_k = r_{k+1} − f_k · d_k;
end for
\\ LSB
d_1 = r_2;
return (d_m d_{m−1} · · · d_1);
```

Like the parallel numeral framework, the Fibonacci-based numeral framework is finished, and in this manner any number v can be spoken to right now. Be that as it may, the Fibonacci-based numeral framework is questionable. For instance, there are six 7-digit vectors in the Fibonacci numeral framework for the decimal number 19: {0111101, 0111110, 1001101, 1001110, 1010001, and 1010010}. For clearness, we allude to a vector in the paired numeral framework as a double vector or twofold code; a vector in the Fibonacci numeral framework is alluded to as a Fibonacci vector or Fibonacci code. All the Fibonacci vectors that speak to a similar worth are characterized as comparable vectors.

The n-bit twofold vector can speak to numbers in the scope of [0, 2n−1], and subsequently an aggregate of 2n qualities can be spoken to by n-bit parallel vectors. we realize that the scope of a m-bit Fibonacci vector is [0, fm+2−1], where the base worth 0 relates to all the bits dk being 0, and the greatest worth compares to all dk being 1. Subsequently an aggregate of fm+2 unmistakable qualities can be spoken to by m-bit Fibonacci vectors. We initially propose a coding plan that changes over the info information to a prohibited example free Fibonacci vector. The code is close ideal since the necessary overhead is close to 1 extra piece, contrasted with the hypothetical lower bound given The coding calculation is created dependent on an outcome that expresses that any number v can be spoken to in FNS, in a FPF way. So as to demonstrate this outcome, we initially determine the

Figure 3 CPF encoding algorithm

accompanying conclusions: The accompanying two m-bit Fibonacci vectors are comparable: dmdm−1 · d301 and dmdm−1 · d310. At the end of the day, dmdm−1 · d301 ≡dmdm−1 · d310.

Evidence Since f2 = f1 = 1, clearly the last two digits are tradable

Figure. 3 show that a m-bit FPF vector is produced in m stages. Each stage yields the slightest bit of the yield vector (dk) and the rest of () that is the contribution to the accompanying stage. In the k[th] arrange the information rk+1 is contrasted with two Fibonacci numbers fk+1 and fk. In the event that rk+1 ≥ fk+1, dk is coded as 1; If rk+1 < fk , dk is coded as 0; If the worth rk+1 is in the middle of, dk is coded to a similar incentive as dk+1. The rest of registered as rk+1 − dk · fk . We will allude the extents [fk+1, fk+2), (fk , fk+1) and [0, fk) as the power 1 zone, hazy area and power 0 zone of the kth organize individually. The most huge piece (MSB) organize is marginally unique in relation to different stages since no bit continues it. It encodes dm by contrasting the information v and only one Fibonacci number, fm+1.

```
Input: d;
  r_m = d;
  for k = m − 1 to 1 do
      if r_{k+1} < f_{2⌈(k−1)/2⌉} then
          c_k = 0;
      else
          c_k = 1;
      end if
      r_k = r_{k+1} − f_{k−1} · c_k;
  end for
  c_0 = r_1;
Output: c_{m−1} c_{m−2} · · · c_0;
```

Fig NFF encoding algorithm

Fig CRF encoding Process

The decoder is a direct usage of Eq. 2 which changes over the Fibonacci vector back to the parallel vector The accuracy of Algorithm can be demonstrated by indicating that if after the kth arrange, the incompletely produced yield vector dm · dk+1dk is FPF, at that point including the yield of the $(k-1)^{th}$ stage, dk−1 won't present an illegal example.

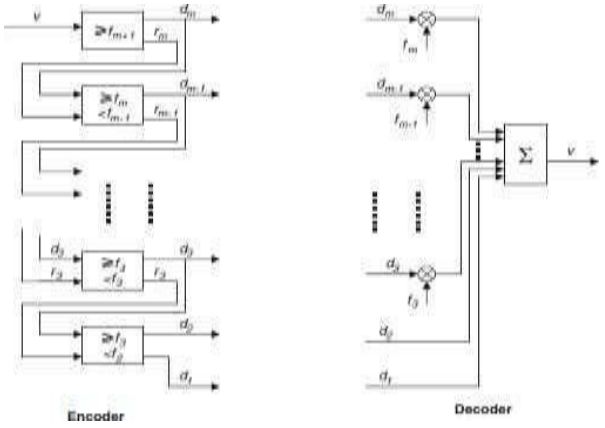


Figure 4 Encoder and Decoder Implementation

Table 7-bit near-optimal FPF code books

Input Decimal value	CODE-1 f_8	f_7	f_6	f_5	f_2	f_1	CODE-2 f_8	f_7	f_6	f_5	f_2	f_1
20*	1	1	1	1	1	1						
19*	1	1	1	1	1	0						
18*	1	1	1	1	0	0						
17*	1	1	1	0	0	1						
16*	1	1	1	0	0	0						
15	1	1	0	0	1	1						
14	1	1	0	0	0	1						
13	1	1	0	0	0	0						
12	0	1	1	1	1	1	1	0	0	1	1	1
11	0	1	1	1	1	0	1	0	0	1	1	0
10	0	1	1	1	0	0	1	0	0	0	1	1
9	0	1	1	0	0	1	1	0	0	0	0	1
8	0	1	1	0	0	0	1	0	0	0	0	0
7	0	0	1	1	1	1						
6	0	0	1	1	1	0						
5	0	0	1	1	0	0						
4	0	0	0	1	1	1						
3	0	0	0	1	1	0						
2	0	0	0	0	1	1						
1	0	0	0	0	0	1						
0	0	0	0	0	0	0						

data-word	Fibonacci codeword $\mathcal{NFF}_4$				$\mathcal{RF}_4$				$\mathcal{CRF}_4$			
4 2 1	5	3	2	1	3	2	1	1	3	2	1	1
0 0 0	0	0	0	0	0	0	0	0	0	0	0	0
0 0 1	0	0	0	1	0	0	0	1	0	0	1	0
0 1 0	0	0	1	0	0	1	0	0	0	0	1	1
0 1 1	0	1	0	0	0	1	0	1	1	0	0	0
1 0 0	0	1	0	1	0	1	1	1	1	0	1	0
1 0 1	1	0	0	0	1	1	0	0	1	0	1	1
1 1 0	1	0	0	1	1	1	0	1	1	1	1	0
1 1 1	1	0	1	0	1	1	1	1	1	1	1	1

Figure 5 FPF Code book & all implementations code book

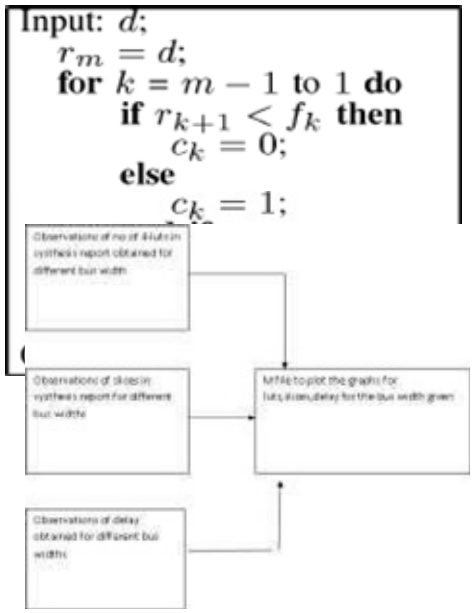


Figure 6 Matlab Design

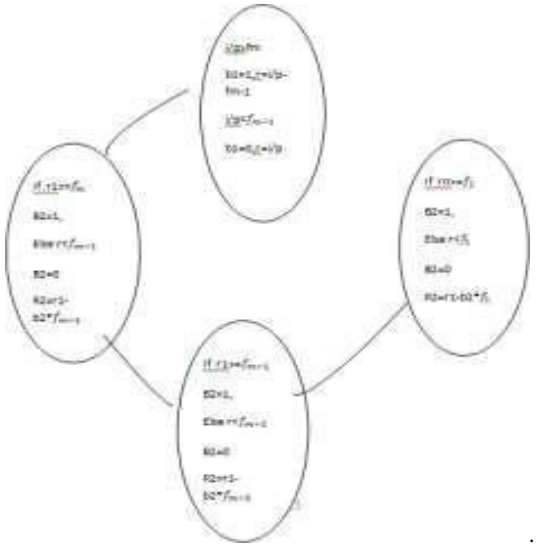


Figure 7 FSM Chart Implementation

IV. RESULTS

We proposed a group of Fibonacci coding procedures for crosstalk evasion by abusing Fibonacci number framework. Figure 8 and 9 Show the Simulated Waveform and RTL schematic of the proposed FTF Codec.

Crosstalk shirking codes are demonstrated to have the option to lessen the between wire crosstalk and in this manner support the most extreme speed on the information transport. They have the benefit of devouring less zone

overhead than protecting systems. Despite the fact that few distinct sorts of codes have been proposed in the previous not many years, no mapping plan was given which encourages the CODEC usage. Intensified by the nonlinear idea of the CAC, the absence of an answer for the efficient development of the CODEC has hampered the wide utilization of CAC practically speaking. Right now, give what we accept is the principal answer for this issue. We indicated that information can be coded to a prohibited example free vector in the Fibonacci numeral framework. We first give a direct mapping calculation that delivers a lot of FPF codes with close ideal cardinality. The territory overhead of this coding plan is close to the hypothetical lower bound. The CODEC dependent on this coding plan is efficient and has extremely low multifaceted nature. The size of the CODEC develops quadratically with the information transport size instead of exponentially in a beast constrained execution. Our foundational coding plan permits the code structure of subjectively enormous transports without depending on transport dividing.

V. CONCLUSIONS

In this paper, we demonstrated the reliance among the proposed methods and gave a proper technique to change over a code word set into another code word set. We likewise related our proposed procedures with a portion of the current crosstalk evasion coding methods. The proposed strategies take out crosstalk totally, however not inductance. The most pessimistic scenario inductance happens when contiguous lines change a similar way. We intend to think of an appropriate instrument to limit the inductance impacts utilizing Fibonacci codes in future.

We can additionally propose an improved coding plan which yields a lot of FPF codes with most extreme cardinality. The zone overhead of this ideal coding plan coordinates the hypothetical lower bound. We gave the comparing change in the CODEC configuration too. This paper additionally talks about issues related with CODEC usage. We proposed an adjusted coding plan that takes out the MSB organize in the encoder and streamlines the decoder side too. The alteration lessens the absolute door check and improves the CODECspeed.

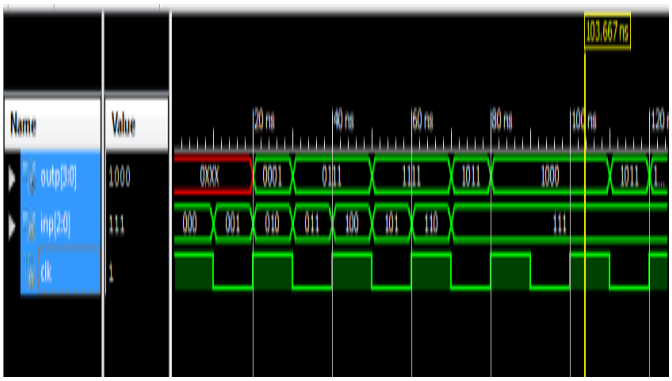


Figure 8 CPF simulation waveform

Figure 9 Nff simulation waveform

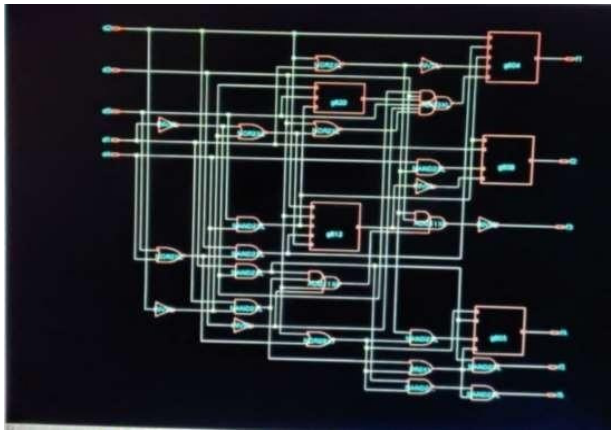


Figure 10 RTL Schematic of the Designed Model

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